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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: August 13, 2001

(use as many sheets as necessary)

Sheet	1	of	3
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Complete if Known

Application Number	To Be Assigned
Filing Dat	August 13, 2001
First Nam d Inv ntor	Andrew J. WALKER et al.
Group Art Unit	Unassigned 2829
Examiner Name	Unassigned PEF
Attorney Docket Number	035905/0103

09/13/01

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
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Considered

Y-19-03

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Sheet 2 of 3		First Named Inventor	Andrew J. WALKER et al.
		Group Art Unit	Unassigned 2029
		Examiner Name	Unassigned Per
		Attorney Docket Number	035905/0103

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
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Examiner Signature		Date Considered	9-18-03
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Date Submitted: August 13, 2001 (use as many sheets as necessary)		Filing Dat	August 13, 2001
Sheet 3 of 3		First Nam d Inv nt r	Andrew J. WALKER et al.
		Group Art Unit	Unassigned
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		Attorney Docket Number	035905/0103

2019 U.S. PTO
09/19/2002
03/13/02

OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS			
Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
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Examiner Signature	<i>Sam Rest</i>	Date Considered	4-18-03
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PTO/SB/08B (08-00)

Approved for through 10/31/2002. OMB 0651-0031

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

Date Submitted: November 26, 2001

References many sheets as necessary)

Sheet 1 of 7

Complete if Known

Application Number	09/927,642
Filing Date	08/13/2001
First Named Inventor	Andrew J. WALKER et al.
Group Art Unit	2818 2829
Examiner Name	Unassigned Per
Attorney Docket Number	035905-0103

U.S. PATENT DOCUMENTS

Examiner Initials*	Citation No.	U.S. Patent Document Number	Kind Code ² (if known)	Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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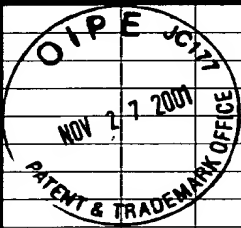
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VICTOR W.C. CHAN et al.: "Three Dimensional CMOS Integrated Circuits on Large Grain Polysilicon Films," IEDM, 2000, IEEE

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EL	A137	JA-HUM KU et al.: "High Performance pMOSFETs With Ni(Si/sub x/Ge/sub 1-x Si/Sub 0.8/Ge/sub 0.2/ gate, IEEE Xplore Citation," VLSI Technology, 2000. Digest of Technical Paper Symposium on page(s): 114-115 June 13-15 2000	
EL	A138	NAE-IN LEE et al.: "High-Performance EEPROM's Using N- and P-Channel Polysilicon Thin-Film Transistors with Electron Cyclotron Resonance N2O-Plasma Oxide," pgs. 15-17, IEEE Electron Device Letters, Vol. 20, No. 1, January 1999, IEEE	
EL	A139	JIN-WOO LEE et al.: "Improved Stability of Polysilicon Thin-Film Transistors under Self-Heating and High Endurance EEPROM Cells for Systems-On-Panel," IEEE Electron Device Letters, 1998, pgs. 265-268, IEEE	
EL	A140	SEOK-WOON LEE et al.: "Pd induced lateral crystallization of Amorphous Si Thin Films," Appl. Phys. Lett. 66 (13), pgs. 1671-1673, 27 March 1995, American Institute of Physics	
EL	A141	K. MIYASHITA et al.: "Optimized Halo Structure for 80 nm Physical Gate CMOS Technology with Indium and Antimony Highly Angled Ion Implantation," IEDM 99-645, pgs. 27.2.1-27.2.4, 1999, IEEE	

Examiner Signature		Date Considered	4-18-03
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¹ Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document.

⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: November 26, 2001 (use as many sheets as necessary)		Applicant Number	09/927,642
		Filing Date	08/13/2001
		First Named Inventor	Andrew J. WALKER et al.
		Group Art Unit	2818 2829
		Examiner Name	Unassigned <i>part</i>
Sheet 6 of 7	Attorney Docket Number	035905-0103	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
<i>EL</i>	A142	N.D. YOUNG et al.: "The Fabrication and Characterization of EEPROM Arrays on Glass Using a Low-Temperature Poly-Si TFT Process," IEEE Transactions on Electron Devices, pgs. 1930-1936, Vol. 43, No. 11, November 1996, IEEE	
<i>EL</i>	A143	JUNG-HOON OH et al.: "A High-Endurance Low-Temperature Polysilicon Thin-Film Transistor EEPROM Cell," pgs. 304-306, IEEE Electron Device Letters, Vol. 21, No. 6, June 2000, IEEE	
<i>EL</i>	A144	M.C. POON. et al.: "Thermal Stability of Cobalt and Nickel Silicides in Amorpho Crystalline Silicon," pg. 1, IEEE Xplore, Electron Devices Meeting, 1997, Proceedings, 19 Hong Kong, 2000, IEEE	
<i>EL</i>	A145	NORIAKI SATO et al.: "A New Programmable Cell Utilizing Insulator Breakdown," IEDM 85, pgs. 639-642, 1985, IEEE	
<i>EL</i>	A146	TAKEO SHIBA et al.: "In Situ Phosphorus-Doped Polysilicon Emitter Technology for Very High-Speed, Small Emitter Bipolar Transistors," IEEE Transactions on Electron Devices, pgs. 889-897, Vol. 43, No. 6, June 1996, IEEE	
<i>EL</i>	A147	SEUNGHEON SONG et al.: "High Performance Transistors with State-of-the-Art CMOS Technologies," IEDM 99, pgs. 427-430, 1999, IEEE	
<i>EL</i>	A148	YOSHIHIRO TAKAO et al.: "Low-Power and High-Stability SRAM Technology Using a Laser-Recrystallized p-Channel SOI MOSFET," IEEE Transactions on Electron Devices, pgs. 2147-2152, Vol. 39, No. 9, September 1992, IEEE	
<i>EL</i>	A149	KENJI TANIGUCHI et al.: "Process Modeling and Simulation: Boundary Conditions for Point Defect-Based Impurity Diffusion Model," IEEE Transactions on Computer-Aided Design, pgs. 1177-1183, Vol. 9, No. 11, November 1990, IEEE	
<i>EL</i>	A150	HONGMEI WANG et al.: "Submicron Super TFTs for 3-D VLSI Applications," IEEE Electron Device Letters, Vol. 21, No. 9, pgs. 439-441, September 2000, IEEE	

Examiner Signature	<i>Enn [Signature]</i>	Date Considered	4-18-03
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,642
Date Submitted: November 27, 2001		Filing Date	08/13/2001
(use as many sheets as necessary)		First Named Inventor	Andrew J. WALKER et al.
		Group Art Unit	2818-2929
		Examiner Name	Unassigned <i>Perf</i>
Sheet	7 of 7	Attorney Docket Number	035905-0103

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

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<i>EL</i>	A151	HONGMEI WANG et al.: "Super Thin-Film Transistor with SOI CMOS Performance Formed by a Novel Grain Enhancement Method," IEEE Transactions on Electron Devices, pgs. 1580-1586, Vol. 47, No. 8, August 2000, IEEE	
<i>EL</i>	A152	MARVIN H. WHITE et al.: "On the Go With Sonos," Circuit & Devices, pgs. 22-31, July 2000, IEEE	
<i>EL</i>	A153	B.J. WOO et al.: "A Novel Memory Cell Using Flash Array Contactless Eprom (Face) Technology," IEDM, pgs. 90-93, 1990, IEEE	
<i>EL</i>	A154	QI XIANG et al.: "Deep sub-100 nm CMOS with Ultra Low Gate Sheet Resist NiSi," VLSI Technology, 2000. Digest of Technical Paper Symposium on... pgs. 76-77, IEEE Xplore, June 13-15, 2000	
<i>EL</i>	A155	QI XIANG et al.: "Deep Sub-100nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," IEEE, pgs. 76-77, 2000, Symposium on VLSI Technology Digest of Technical Papers	
<i>EL</i>	A156	QIUXIA XU et al.: "New Ti-SALICIDE Process Using Sb and Ge Preamorphization for Sub-0.2 μ m CMOS Technology," IEEE Transactions on Electron Devices, pgs. 2002-2009, Vol. 45, No. 9, September 1998, IEEE	
<i>EL</i>	A157	KUNIYOSHI YOSHIKAWA et al.: "An Asymmetrical Lightly Doped Source Cell for Virtual Ground High-Density EPROM's," IEEE Transactions on Electron Devices, pgs. 1046-1051, Vol. 37, No. 4, April 1990, IEEE	
<i>EL</i>	A158	QI XIANG et al.: "Deep Sub-100nm CMOS with Ultra Low Gate Sheet Resistance by NiSi," pgs. 76-77, 2000 Symposium on VLSI Technology Digest of Technical Papers	
<i>EL</i>	A159	VIVEK SUBRAMANIAN: "Control of Nucleation and Grain Growth in Solid-Phase Crystallized Silicon for High-Performance Thin Film Transistors," A Dissertation submitted to the Department of Electrical Engineering and the Committee of Graduate Studies of Stanford University, 1998	
<i>EL</i>	A160	DIETMAR GOGL et al.: "A 1-Kbit EEPROM in SIMOX Technology for High-Temperature Applications up to 250° C," IEEE Journal of Solid-State Circuits, October 2000, Vol. 35, No. 10, IEEE	

Examiner Signature	<i>EL</i>	Date Considered	4-18-03
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Substitute for form 1449B/PTO		Complete if Known	
INFORMATION DISCLOSURE STATEMENT BY APPLICANT		Application Number	09/927,642
Date Submitted: April 1, 2002		Filing Date	08/13/2001
(use as many sheets as necessary)		First Named Inventor	Andrew J. WALKER et al.
		Group Art Unit	2818 2829
		Examiner Name	Unassigned per T
Sheet	1 of 1	Attorney Docket Number	035905-0103

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
EP	A161	6,208,545		Leedy	3/27/2001	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

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Examiner Signature	<i>Eva Perot</i>	Date Considered	7-18-03
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Substitute for form 1449B/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Date Submitted: June 27, 2002

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Sheet 1 of 1

Complete if Known

Application Number	09/927,642
Filing Date	08/13/2001
First Named Inventor	Andrew J. Walker al.
Group Art Unit	2818 2829
Examiner Name	Not Assigned Pert
Attorney Docket Number	035905-0103

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
EP	C1	5,283,468		Kondo	FE-01-1994	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

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EP	C2	"3D Chip-On-Chip Stacking", Semiconductor International, December 1991.	
EP	C3	LAY, RICHARD, "TRW Develops Wireless Multiboard Interconnect System", Electronic Engineering Times, November 5, 1994.	

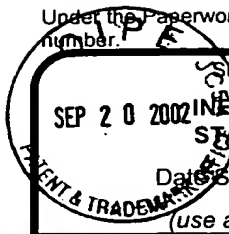
Examiner Signature	Evan Pert	Date Considered	4-18-03
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Application Number	09/927,642	Filing Date	08/13/2001
First Named Inventor	Andrew J. WALKER et al.	Group Art Unit	2848 2829
Examiner Name	Unassigned <i>Perf</i>	Attorney Docket Number	035905-0103

U.S. PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
<i>EP</i>	B1	5,973,356		Noble	10/26/1999	
<i>EP</i>	B2	0055838A1		Walker, et al	12/27/2001	
<i>EP</i>	B3	0028541A1		Lee, et al	03/07/2002	

FOREIGN PATENT DOCUMENTS								
Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				

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Examiner Signature	<i>Evan Perf</i>	Date Considered	4-18-03
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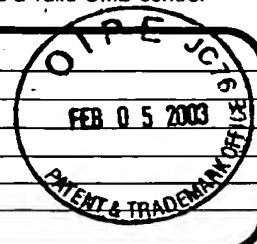
Date Submitted: **02-05-03**

(use as many sheets as necessary)

Sheet **1** of **1**

Complete if Known

Application Number **09/927,642**
 Filing Date **08/13/2001**
 First Named Inventor **Andrew J. Walker**
 Group Art Unit **2829**
 Examiner Name **Evan T. Pert**
 Attorney Docket Number **035905-0103**



U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			

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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
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EP	B4	WADA Y. et al., "Active-Body-Bias SOI-CMOS Driver Circuits", June 1997 Symposium on VLSI Circuits Digest of Technical Papers, pages 29-30	Y

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Signature

Evan Pert

Date
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4-18-03

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Substitute for form 1449B/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT Date Submitted: June 11, 2002 Use as many sheets as necessary		Complete if Known	
Application Number		09/927,462	
Filing Date		08/13/2001	
First Named Inventor		Andrew J. WALKER et al.	
Group Art Unit		2818 2829	
Examiner Name		Unassigned Per	
Attorney Docket Number		035905-0103	

U.S. PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
EP	B1	4,500,905		Shibata		
EP	B2	6,185,122		Johnson et al.		
EP	B3	3,414,892		McCormack et al.	12/13/1968	
EP	B4	3,432,827		Sarno	3/11/1969	
EP	B5	4,535,424		Reid		
EP	B6	4,630,096		Drye		
EP	B7	4,672,577		Hirose		
EP	B8	4,710,798		Marcantonio		
EP	B9	4,811,082		Jacobs		
EP	B10	5,001,539		Inoue et al.		
EP	B11	5,089,862		Warner, Jr. et al.		
EP	B12	5,160,987		Pricer et al.		
EP	B13	5,191,405		Tomita et al.		
EP	B14	5,202,754		Bertin et al.		
EP	B15	5,266,912		Kledzik		
EP	B16	5,283,458		Stokes et al.		
EP	B17	5,398,200		Mazure et al.		
EP	B18	5,422,435		Takiar et al.		
EP	B19	5,426,566		Beilstein, Jr		
EP	B20	5,434,745		Shokrgozar et al.		
EP	B21	5,453,952		Okudaira		
EP	B22	5,455,455		Kurtz et al.		
EP	B23	5,468,997		Imai et al.		
EP	B24	5,471,090		Deutsch		
EP	B25	5,481,133		Hsu		
EP	B26	5,495,398		Takiar et al.		
EP	B27	5,502,289		Takiar et al.		
EP	B28	5,523,622		Harada et al.		
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EP	B33	5,585,675		Knopf		
EP	B34	5,612,570		Eide et al.		
EP	B35	5,654,220		Leedy		
EP	B36	5,693,552		Hsu		
EP	B37	5,696,031		Wark		
EP	B38	5,703,747		Voldman et al.		
EP	B39	5,780,925		Cipolla et al.		
EP	B40	5,781,031		Bertin et al.		
EP	B41	5,801,437		Burns		
EP	B42	5,915,167		Leedy		

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Evan Per

Date Considered

4-18-03

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<div style="border: 2px solid black; border-radius: 50%; padding: 10px; display: inline-block; text-align: center;"> DIPE J JUN 11 2002 PATENT & TRADEMARK </div> <p style="text-align: center;">Substitute for form 1449B/PTO</p> <p style="text-align: center;">INFORMATION DISCLOSURE STATEMENT BY APPLICANT</p> <p style="text-align: center;">Date Submitted: June 11, 2002</p> <p style="text-align: center;">(use as many sheets as necessary)</p> <p style="text-align: center;">2 of 7</p>	<p style="text-align: right;">Complete if Known</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 60%;">Application Number</td> <td>09/927,462</td> </tr> <tr> <td>Filing Date</td> <td>08/13/2001</td> </tr> <tr> <td>First Named Inventor</td> <td>Andrew J. WALKER et al.</td> </tr> <tr> <td>Group Art Unit</td> <td>2848 2829</td> </tr> <tr> <td>Examiner Name</td> <td>Unassigned <i>Per +</i></td> </tr> <tr> <td>Attorney Docket Number</td> <td>035905-0103</td> </tr> </table>	Application Number	09/927,462	Filing Date	08/13/2001	First Named Inventor	Andrew J. WALKER et al.	Group Art Unit	2848 2829	Examiner Name	Unassigned <i>Per +</i>	Attorney Docket Number	035905-0103
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		U.S. Patent Document			
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Examiner Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Documents	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Office ³	Number ⁴	Kind Code ⁵ (if known)				
SP	B60	EPO	0 073 486	A2	Toyama et al.	8-26-1982		
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Examiner Signature	<i>Walker +</i>	Date Considered	<i>4-18-03</i>
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		Group Art Unit	2818 2829
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		Attorney Docket Number	035905-0103

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
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Examiner Signature	<i>Eugene Per X</i>	Date Considered	4-18-03
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Sheet 4	of 7	Attorney Docket Number	035905-0103

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.) date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ⁶
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<i>EP</i>	B118	Patent Application, FUJIMOTO et al, US 2002/0027275 A1.	

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Sheet 7 of 7

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